**What is Claimed is:**

1. A tag array memory comprising:

an input conversion circuit to receive a 1-hot vector and to convert the 1-hot vector to a 2-hot vector;

a memory array coupled to the input conversion circuit, the memory array to store the 2-hot vector; and

an output conversion circuit coupled to the memory array, the output conversion circuit to receive the 2-hot vector and to convert the 2-hot vector back to the 1-hot vector.

2. The tag array memory of claim 1 wherein the memory array comprises:

a plurality of memory cells wherein each memory cell comprises:

a plurality of memory bit circuits coupled together, each of the plurality of memory bit circuits having a plurality of blind invalidate circuits, each blind invalidate circuit being coupled to a left neighbor bit circuit and a right neighbor bit circuit, and each blind invalidate circuit to check a bit value of the right neighbor memory bit circuit and a bit value of the left neighbor memory bit circuit.

3. The tag array memory of claim 2 wherein each of the plurality of blind invalidate circuits comprises:

a primary clear bit line;

a primary clear circuit coupled to the primary clear bit line to receive a bit value of a left-adjacent memory bit circuit; and

an auxiliary clear circuit coupled to the primary clear circuit and to the primary clear circuit of a right-adjacent memory bit circuit, the auxiliary clear circuit to receive a bit value of the right-adjacent memory bit circuit.

4. The tag array memory of claim 3 wherein the primary clear circuit is to clear the bit in the memory bit circuit if the primary clear bit line is asserted and the bit value of the right-adjacent memory bit circuit is zero.

5. The tag array memory circuit of claim 4 wherein the auxiliary clear circuit is to clear the bit in the memory bit circuit, if the primary clear bit line is asserted and the bit value of the left-adjacent memory bit circuit is zero.

6. The tag array memory circuit of claim 4 wherein the primary clear circuit is to clear the bit in the memory bit circuit in a single clock cycle.

7. The tag array memory of claim 3 wherein the auxiliary clear circuit is to clear the bit in the memory bit circuit if the primary clear bit line is asserted and the bit value of the left-adjacent memory bit circuit is zero.

8. The tag array memory circuit of claim 7 wherein the auxiliary clear circuit is to clear the bit in the memory bit circuit in a single clock cycle.

9. The tag array memory of claim 1 wherein the input conversion circuit is further coupled to a translation look-aside buffer.

10. The tag array memory of claim 9 wherein the input conversion circuit is to receive the 1-hot vector from the translation look-aside buffer.

11. The tag array memory of claim 9 wherein the memory array is to receive the two-hot vector from the input conversion circuit and an index value.

12. The tag array memory of claim 11 wherein the index value is received from an incoming tag cache access address request.

13. The tag array memory of claim 1 further comprising:

a plurality of comparators coupled to the output conversion circuit.

14. The tag array memory of claim 13 wherein the plurality of comparators are further coupled to the translation look-aside buffer to receive the 1-hot vector.

15. The tag array memory of claim 14 further comprising:

a first multiplexer coupled to the plurality of comparators and coupled to a cache data array.

16. The tag array memory of claim 15 further comprising:

a second multiplexer coupled to the first multiplexer, the second multiplexer to receive data from the cache data array and a byte select value.

17. The tag array memory of claim 16 wherein said second multiplexer is to output a byte value using the byte select value.

18. A computer system, comprising:

a processor;

a translation look-aside buffer (TLB); and

a tag array memory coupled to the TLB, the tag array memory comprising:

an input conversion circuit to receive a 1-hot vector and to convert the 1-hot vector to a 2-hot vector;

a memory array coupled to the input conversion circuit, the memory array to store the 2-hot vector; and

an output conversion circuit coupled to the memory array, the output conversion circuit to receive the 2-hot vector and to convert the 2-hot vector back to the 1-hot vector.

19. The computer system of claim 18 wherein the memory array comprises:

a plurality of memory cells wherein each memory cell comprises:

a plurality of memory bit circuits coupled together, each of the plurality of memory bit circuits having a plurality of blind invalidate circuits, each blind invalidate circuit being coupled to a left neighbor bit circuit and a right neighbor bit circuit, and each blind invalidate circuit to check a bit value of the right neighbor memory bit circuit and a bit value of

the left neighbor memory bit circuit.

20. The computer system of claim 19 wherein each of the plurality of blind invalidate circuits comprises:

a primary clear bit line;

a primary clear circuit coupled to the primary clear bit line to receive a bit value of a left-adjacent memory bit circuit; and

an auxiliary clear circuit coupled to the primary clear circuit and to the primary clear circuit of a right-adjacent memory bit circuit, the auxiliary clear circuit to receive a bit value of the right-adjacent memory bit circuit.

21. The computer system of claim 20 wherein the primary clear circuit is to clear the bit in the memory bit circuit if the primary clear bit line is asserted and the bit value of the right-adjacent memory bit circuit is zero.

22. The tag array memory of claim 20 wherein the auxiliary clear circuit is to clear the bit in the memory bit circuit if the primary clear bit line is asserted and the bit value of the left-adjacent memory bit circuit is zero.

23. A method comprising:

receiving a 1-hot vector;

converting the 1-hot vector to a 2-hot vector;

storing the 2-hot vector; and

invalidating the 2-hot vector, if the 1-hot vector becomes invalid.

24. The method of claim 23 wherein converting the 1-hot vector to a 2-hot vector, comprises:

determining a primary bit in the 1-hot vector, the primary bit being the bit with a value of 1; and

adding a 1 to a neighbor bit of the primary bit.

25. The method of claim 24 wherein the neighbor bit is immediately to the left of the primary bit.

26. The method of claim 24 wherein storing the 2-hot vector comprises:

writing the 2-hot vector to a memory.

27. The method of claim 26 wherein writing the 2-hot vector to a memory comprises:

writing the 2-hot vector to a cache.

28. The method of claim 23 wherein invalidating the 2-hot vector, if the 1-hot vector becomes invalid, comprises:

converting the invalid 1-hot vector to an invalid 2-hot vector; and

clearing each occurrence of the invalid 2-hot vector.

29. The method of claim 28 wherein for each invalid 2-hot vector, clearing each occurrence of the invalid 2-hot vector comprises:

setting the primary bit equal to zero; and

setting the neighbor bit equal to zero.

30. A machine-readable medium having stored thereon instructions to perform a method comprising:

receiving a 1-hot vector;

converting the 1-hot vector to a 2-hot vector;

storing the 2-hot vector; and

invalidating the 2-hot vector, if the 1-hot vector becomes invalid.

31. The machine-readable medium of claim 30 wherein converting the 1-hot vector and a valid bit to a 2-hot vector, comprises:

determining a primary bit in the 1-hot vector, the primary bit being the bit with a value of 1; and

adding a 1 to a neighbor bit of the primary bit.

32. The machine-readable medium of claim 31 wherein the neighbor bit is immediately to the left of a primary bit.

33. The machine-readable medium of claim 31 wherein storing the 2-hot vector, comprises:

writing the 2-hot vector to a memory.

34. The machine-readable medium of claim 33 wherein writing the 2-hot vector to a memory comprises:

writing the 2-hot vector to a cache.

35. The machine-readable medium of claim 30 wherein invalidating the 2-hot vector, if the 1-hot vector becomes invalid, comprises:

converting the invalid 1-hot vector to an invalid 2-hot vector; and

clearing each occurrence of the invalid 2-hot vector.

36. The machine-readable medium of claim 35 wherein for each invalid 2-hot vector, clearing each occurrence the invalid 2-hot vector comprises:

setting the primary bit equal to zero; and

setting the neighbor bit equal to zero.